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PATENT NUMBER

 11/11/00 8. PTO  
 09/808339  
 03/13/01

Class	Subclass	ISSUE CLASSIFICATION

## U.S. UTILITY Patent Application

O.I.P.E. SCANNED <i>82</i> O.A. <i>LR</i>	PATENT DATE
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APPLICATION NO. 09/808339	CONT/PRIOR D	CLASS 706	SUBCLASS 14	ART UNIT 2122	EXAMINER PHAN, THAI
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 APPLICANTS  
 Yo Ng Zhou  
 Antony Fan

2128

 TITLE  
 System and method for simulation of an integrated circuit design using a hierarchical input netlist and divisions along hierarchical boundaries thereof
PTO-2040  
12/99

## ISSUING CLASSIFICATION

ORIGINAL		CROSS REFERENCE(S)					
CLASS	SUBCLASS	CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)				
INTERNATIONAL CLASSIFICATION							

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<input type="checkbox"/> <b>TERMINAL DISCLAIMER</b>  <input type="checkbox"/> The term of this patent subsequent to _____ (date) has been disclaimed.  <input type="checkbox"/> The term of this patent shall not extend beyond the expiration date of U.S. Patent. No. _____  <input type="checkbox"/> The terminal _____ months of this patent have been disclaimed.	<b>DRAWINGS</b> Sheets Drwg.    Figs. Drwg.    Print Fig.			<b>CLAIMS ALLOWED</b> Total Claims    Print Claim for O.G.	
	_____ (Assistant Examiner)    _____ (Date)			<b>NOTICE OF ALLOWANCE MAILED</b> _____	
	_____ (Primary Examiner)    _____ (Date)			<b>ISSUE FEE</b> Amount Due    Date Paid	
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